## **Low-Power SPI (LPSPI) Module Summary for the S32K3 Board**

### **1. General Structure of the LPSPI Module**

Operates as a controller or peripheral device; features a 32-bit shift register, multiple FIFO buffers, and configurable timing parameters. Key components:

* Configuration Registers: Define operating modes and SPI parameters.
* Command/TX FIFO: Stores transmit commands and data.
* RX FIFO: Holds received data.
* Shift Register: Serializes and deserializes data between controller and peripheral.
* Clock Control: Determines SPI clock phase, polarity, and speed.

Reference: Section 70.2.1, Figure 388 (Block Diagram), Page 2848

### **2. Required Registers and Their Configuration**

#### **2.1 Control Register (CR) - Address: 0x10**

* Module Enable (MEN) [Bit 0]: Enables the LPSPI module. Set to 1 to activate SPI functionality.
  + Configuration: CR |= (1 << 0);
* Software Reset (RST) [Bit 1]: Resets all internal logic and registers except the control register itself.
  + Configuration: CR |= (1 << 1); (write 0 to clear the reset)
* Reset Receive FIFO (RRF) [Bit 8]: Clears the receive FIFO buffer.
  + Configuration: CR |= (1 << 8);
* Reset Transmit FIFO (RTF) [Bit 9]: Clears the transmit FIFO buffer.
  + Configuration: CR |= (1 << 9);

Reference: Section 70.6.1.4, Page 2865

#### **2.2 Status Register (SR) - Address: 0x14**

* Module Busy Flag (MBF) [Bit 24]: Indicates whether the SPI module is actively transferring data. Read-only.
* Transmit Data Flag (TDF) [Bit 0]: Signals that data can be written to the transmit FIFO.
  + Check if TX FIFO is ready: while (!(SR & (1 << 0)));
* Receive Data Flag (RDF) [Bit 1]: Indicates that data is available in the receive FIFO.
  + Check if RX FIFO has data: while (!(SR & (1 << 1)));

Reference: Section 70.6.1.5, Page 2867

#### **2.3 Configuration Register 1 (CFGR1) - Address: 0x24**

* Master Mode (MASTER) [Bit 0]: Configures the LPSPI as a controller (1) or peripheral (0).
  + Enable Controller mode: CFGR1 |= (1 << 0);
* Clock Polarity (CPOL) & Clock Phase (CPHA) [Bits 30-29]: Defines the SPI clock behavior.
  + Set CPOL = 1, CPHA = 1: TCR |= (1 << 30) | (1 << 29);
* Peripheral Chip Select Polarity (PCSPOL) [Bits 15-8]: Defines active-high or active-low chip select signals.
  + Set PCS[0] active-low: CFGR1 &= ~(1 << 8);

Reference: Section 70.6.1.9, Page 2875

#### **2.4 Clock Configuration Registers (CCR & CCR1) - Address: 0x40, 0x44**

* SCK Setup Phase (SCKSET) [Bits 7-0]: Defines the time for which SCK stays high or low.
  + Set SCK high for 5 cycles: CCR1 = (5 << 0);
* PCS to SCK Delay (PCSSCK) [Bits 23-16]: Sets the delay from PCS assertion to the first clock edge.
  + Set PCS-SCK delay to 4 cycles: CCR |= (4 << 16);

Reference: Section 70.6.1.10, Page 2879

### **3. Implementation Notes**

* FIFO Management: LPSPI features a 4-word FIFO for both transmission and reception. The TX FIFO should be refilled whenever TDF is set, and the RX FIFO should be read whenever RDF is set.
* DMA Support: Direct Memory Access (DMA) is available for efficient SPI data transfer by configuring the DMA Enable (DER) register.
* Interrupts: LPSPI supports multiple interrupt sources, including transmit completion (TCIE), frame completion (FCIE), and data match (DMIE).